for a PMOS process. The substrate 10 has an ejection element 20 disposed over the substrate with an intervening field oxide layer 12 providing thermal isolation of the ejection element 20 to the substrate 10. Optionally, additional deposited oxide layers may be disposed on the field oxide layer 12. The ejection element 20 is coupled to a transistor 30, preferably an N-MOS transistor, formed in the substrate 10. The coupling is preferably done using a conductive layer 21, such as aluminum, although other conductors can be used such as copper and gold, to name a couple. The transistor 30 includes a source active region 18 and a drain active region 16 and a gate 14. The ejection element 20 is made from a resistive conductive layer 19 that is deposited on the field oxide layer 12. The area of an opening in the conductive layer 21 defines the ejection element 20. To protect the ejection element 20 from the reactive qualities of fluid to be ejected, such as ink, a passivation layer 22 is disposed over the ejection element 20 and other thin-film layers that have been deposited on the substrate 10. To create a printhead, the integrated circuit [15]11 is combined with an orifice layer 82, shown as a fluid barrier 26 and an orifice plate 28. The ejection element 20 and the passivation layer 22 are protected from damage due to bubble collapse in fluid chamber 92 after fluid ejection from nozzle 90 by a cavitation layer 24 that is disposed over passivation layer 22. The stacks of thin-film layers 32 that are disposed on substrate 10 are those layers processed on the substrate 10 before applying the orifice layer 82. Optionally, the orifice layer 82 can be a single or multiple layer(s) of polymer or epoxy material. Several methods for creating the orifice layer are known to those skilled in the art.

Please change the paragraph starting on page 10, line 7 with the following:

Fig. 7 is an exemplary flow chart of a process used to create an integrated circuit that embodies aspects of the invention. In block 310, the process begins with a doped substrate, preferably a p- doped substrate for N-MOS, and an n-doped substrate for PMOS. In a conventional process, the major steps of

defining active areas and growing field oxide would be performed. In the process of the invention, the conventional steps of defining of the active areas with an active mask and field oxide growth are eliminated. In block 312, a first dielectric layer of gate oxide is applied on the doped substrate. Preferably, a layer of silicon dioxide is formed to create the gate oxide. Alternatively, the gate oxide can be formed from several layers such as a layer of silicon nitride and a layer of silicon dioxide. Additionally, several different methods of applying the gate oxide are known to those skilled in the art. In block 314, a first conductive layer is applied, preferably a deposition of polycrystalline silicon (polysilicon), and patterned with the gate mask and wet or dry etched in block 316 in closed-loop structures to form the gate regions from the remaining first conductive layer, the drain of the transistors formed within the closed-loop and the source of the transistors in the area outside of the closed-loop structures. In block 318, a dopant concentration is applied in the areas of the substrate that is not obstructed by the first conductive layer to create the active regions of the transistors. A substantial portion of the substrate surface will be created as active region because no island mask is used. In block 320, a second dielectric layer, preferably phosphosilicate glass (PSG) is applied to a predetermined thickness (at least 2000 but preferably between about 6000 to about 12,000 Angstroms or greater) to provide sufficient thermal isolation between a later formed ejection element and the substrate 110. Preferably, after the PSG is applied, it is densified. Optionally, before applying the second dielectric layer, a thin layer of thermal oxide can be applied over the source, drain and gate of the transistor, preferably to a thickness of about 50 to 2,000 Angstroms but preferably 1000 Angstroms. In block 322, a first set of contact regions is created in the second dielectric layer using the contact mask to form openings to the first conductive layer and/or the active regions of the transistors. Optionally in block 317, a second etch step is used with the optional substrate contact mask to pattern and etch substrate body contacts. In block 324, a second conductive layer, preferably an electrically resistive layer such as tantalum aluminum, is applied by deposition. Optionally, the second conductive layer is formed of

polycrystalline silicon (polysilicon). The second conductive layer is used to create the ejection element. In block 326, a third conductive layer, such as aluminum, is applied, preferably by deposition or sputtering. In block 328 the third conductive layer is patterned with the metal1 mask and etch to form metal traces for interconnections. The third conductive layer is used to connect the active regions of the transistors to the ejection elements. The third conductive layer is also used to connect various signals from the first conductive layer to active area regions. To convert the integrated circuit to a printhead further steps combine printhead thin-film protective materials and a conductive layer to interface with the integrated circuit thin-films. In block 330, a layer of passivation is applied over the previously applied layers on the substrate. In block 332, using the via mask, the passivation layer is patterned and etched to create a second set of contact regions in the passivation layer to the third conductive layer. Preferably the protective passivation layer is made up of a layer of silicon nitride and a layer of silicon carbide. In block 334, a protective cavitation layer is applied, preferably tantalum, tungsten, or molybdenum. In block 336, the cavitation layer is patterned with the cavitation mask and etched. In block 338, a fourth conductive layer, preferably gold, deposited or sputtered. The fourth conductive layer is patterned with the metal2 mask in block 340 and etched to create conductive traces. The fourth conductive layer traces are used to make contact with the third conductive layer through the second set of contact regions in the passivation layer. External signals to operate the printhead make contact to the fourth conductive layer. In step 342, an orifice layer is applied over the surface of the previously applied stack of thin-film layers on the substrate. The orifice layer is made of one or more layers. One option is to provide a protective barrier layer to define fluid wells (fluid receiving cavities) coupled to the ejection elements, and then applying an orifice plate with nozzles defined therein over the fluid wells for directing any ejected fluid from the printhead. Another option is to apply a photolithographic polymer or epoxy material that can be exposed and developed to form the fluid well and nozzles. The polymer or epoxy material can be made of one or more layers.

Please replace the paragraph beginning on page 9, line 15 with the following:

Fig. 6 is an exemplary schematic illustrating an electrical interface between a recording device and an integrated circuit that combines a transistor 130 with an ejection element 120. In this example, no substrate contact to ground potential is made. The bulk [127] of transistor 130 is shown as having an inherent diode 13 between the bulk [127] and the source 118 connections. In this example, the drain 116 of transistor 130 is coupled to an ejection element 120, a heater resistor. The heater resistor is further connected to a primitive [signal interface]driveline 46. A primitive is a grouping of ejection elements, such as a column of one color in printhead. Thus, the primitive signal interface 46, the gate 114 of the transistor 130 and the source 118 of the transistor 130 form external interface ports (such as contacts 214 in Fig. 9) that a recording device can control. The recording device 240 (see Fig. 10) includes a primitive select circuit 58 that controls power 56 via a switch 60 to preferably a group of ejection elements (a primitive) on the integrated circuit 200 (see Fig. 8). The recording device 240 also includes an address select circuit 66 that interfaces to a driver 62 that selects an individual ejection element within a primitive.

In the Claims:

1. (Amended) An integrated circuit for a printhead, comprising:

a substrate;

a set of transistors formed in the substrate wherein the gate of each of the set of transistors forms at least one closed loop; and

an ejection element coupled to at least one of the set of transistors wherein the ejection element is disposed over the substrate without an intervening field oxide layer.